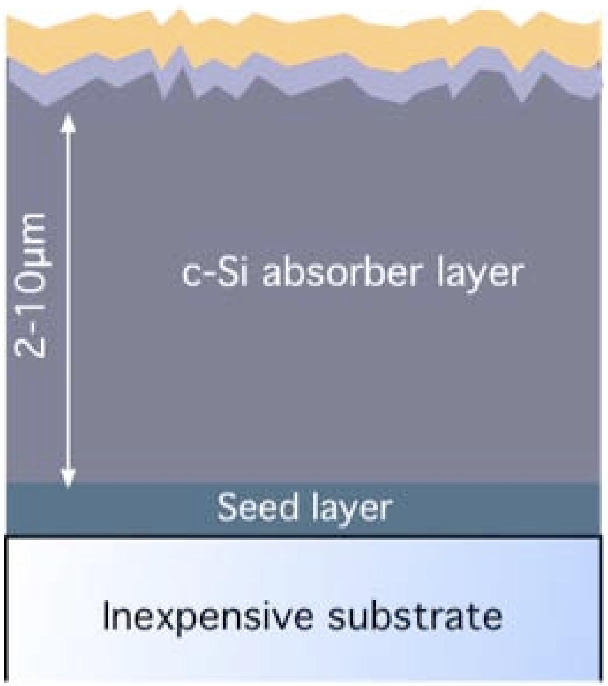


NREL
NATIONAL RENEWABLE ENERGY LABORATORY

NREL Film Silicon Agreement

PV Program Team

P.I. Howard M. Branz
National Renewable Energy Laboratory
1617 Cole Blvd, Golden, CO 80401
howard.branz@nrel.gov
May 26, 2010

Overview: Film Silicon Ageement

U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

Timeline

- Review period of 14 months:
  March 2009 – April 2010
- Funded project end: Sept 30, 2010
- ~ 75% complete

Budget

- Total project funding in review
  - DOE: $3862k for 14 months

- Total FY09 Funds: $3225k
- Total FY10 Funds: $3395k

Barriers

- High cost of wafers in dominant silicon PV technology
- Low efficiency of thin-film PV
- Non-Si PV may face shortages and high prices of key elements (e.g. Te, In, Ga) at TW penetration

Partners

- Project lead: NREL
- Key collaborations
  - Ampulse
  - Corning
  - Sharp Laboratories of America
  - Uni-Solar
  - Xunlight
  - Other industry (proprietary)
  - Oak Ridge National Laboratory
  - Stanford University
  - Columbia University

Challenges, Barriers or Problems

- The PV challenge: TW-scale deployment
  - Requires abundant, non-toxic materials
  - Requires high-quality materials on low-cost substrates
  - Requires 50 to 80 cents/W module cost
    - Efficiency of crystal-Si (15%) at thin-film manufacturing costs (<$100/m^2)
- The advantages of silicon
  - Abundant, non-toxic, well-understood, semiconductor
  - Industrial equipment from PV, IC and a-Si TFT industries
- The key mid-term technical challenge for silicon PV
  - Eliminate the Si Wafer
    - Wafer is ½ the Si module cost today, despite feedstock cost reductions
    - Embedded energy content repaid only after 2-year deployment

Expensive & energy-intensive wafer production

Sand

Add Carbon & Energy

CO_2

Metallurgical grade Si

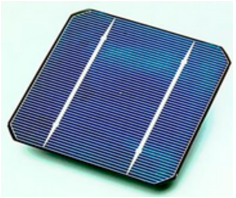
Pure $SiHCl_3$ or SiH_4

Add Heat Energy (1000 °C)

Feedstock

Add more heat energy (1500°C)

Waste ~1/2 in sawing



Use 20X more SI than needed

Film Si decreases materials and energy costs

Sand

Add Carbon & Energy

CO_2

Metallurgical grade Si

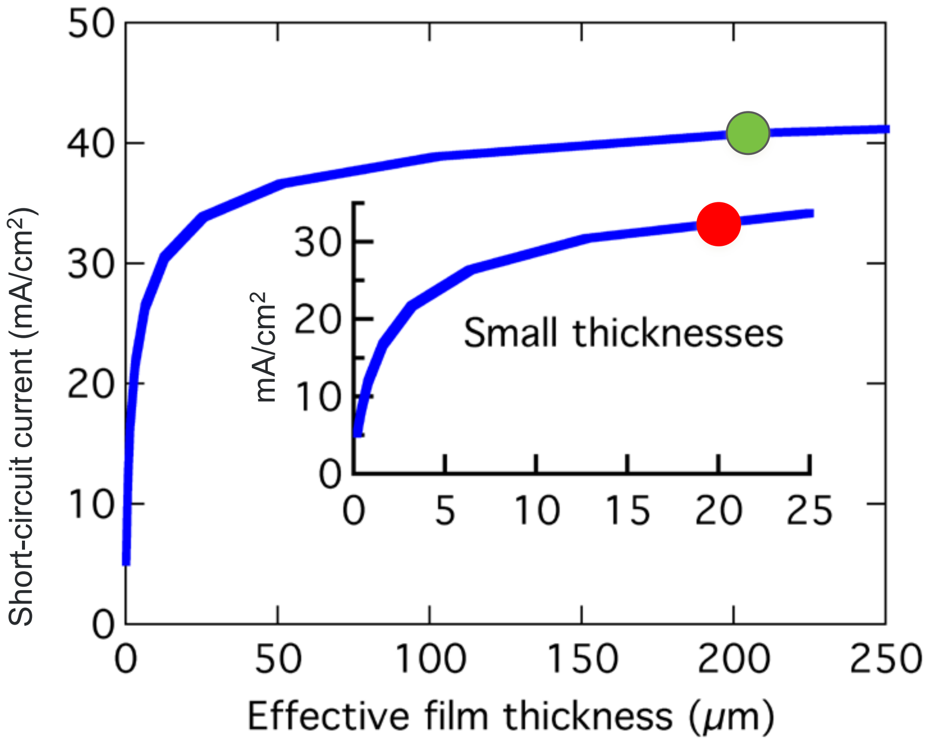
Pure $SiHCl_3$ or SiH_4

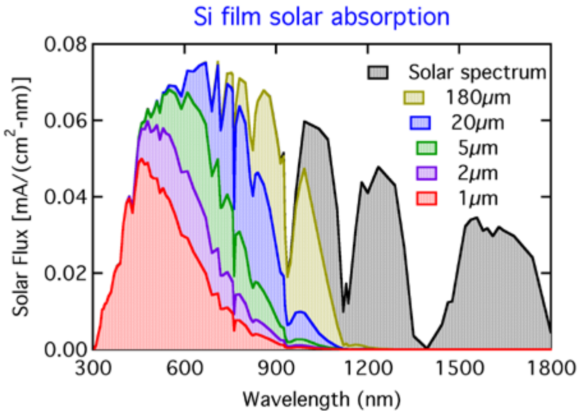
Directly deposit from purest precursor at high rate

Film Silicon PV
Inexpensive substrate

Relevance: With light-trapping, c-Si film can provide needed current for 15% cells

- CSG (Q-Cells) mini-modules: J_{sc}=29.3 mA/cm^2 from 1.85 μm thick c-Si
  - Poor quality, 1-micron grain, recrystallized Si limits efficiency
- Near-term goal: 30 mA/cm^2 from 4-μm c-Si
  - 5X light trapping





Overview of Film Silicon Agreement

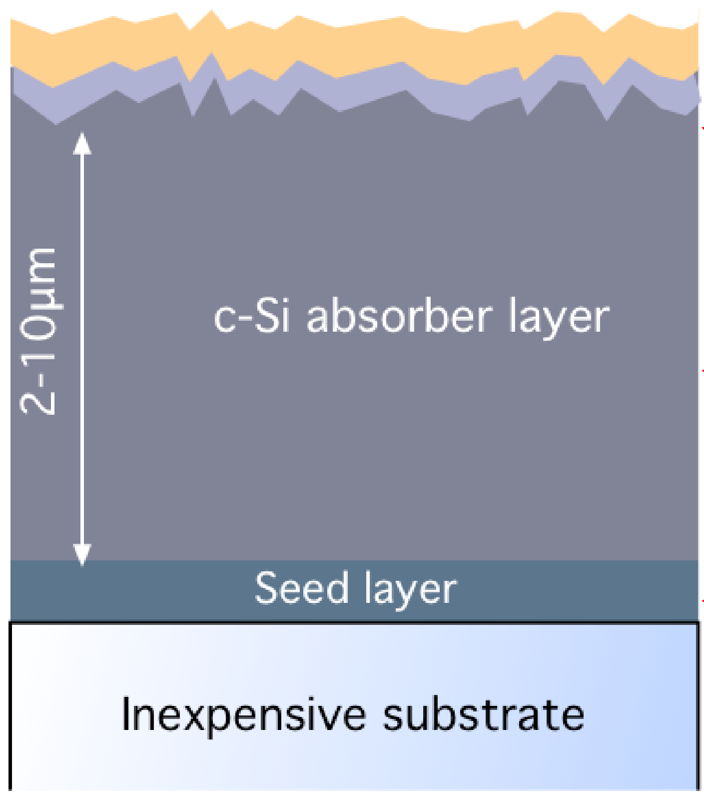
U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

Near-term: thin-film a-Si/nc-Si

- Task: Improve high deposition-rate nc-Si

Goal: increase efficiency and lower capital costs

Mid-term: film c-Si for wafer replacement



New FY09 Task
Devices & models

3 Main Tasks
Improved quality of epitaxial Si at high-rate and low T

3 Small Tasks
Inexpensive crystalline seed layers

Objectives and key tasks FY09 – FY10

U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

- Address most critical needs for >15%-efficient mid-term film crystal silicon
  - Improve high-rate, scalable, hot-wire CVD epitaxy at glass-compatible temperatures
  - Improve rapid thermal anneal and hydrogen passivation
  - Test epitaxy on most promising crystalline seeds on inexpensive substrates
  - Design and fabricate test solar cells to validate epitaxial Si quality
  - PC1D and analytic models of devices to understand limiting physics
  - Plan light-trapping task to begin in FY11
  - Establish firm scientific knowledge for all technologies required

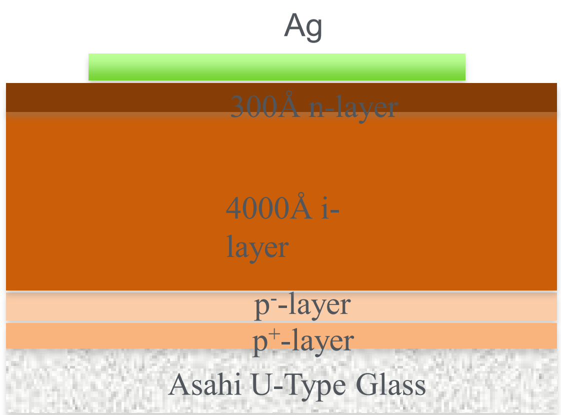
- High-rate nanocrystalline Si for near-term PV use
  - High efficiency hot-wire and VHF CVD a-Si:H and nc-Si devices on 6-inch substrates from PDIL tool
  - Support of U.S. industry
    - Collaborative research with established and startup U.S. companies in film Si PV and new substrates
    - Provide amorphous silicon films to university groups for novel nanostructured, plasmonic and other devices

- All research tasks support goals of DOE Film Silicon Roadmap
  - Key “Technical Improvement Opportunities” for materials and device development addressed
  - Manufacturing equipment and scale left to industrial partners

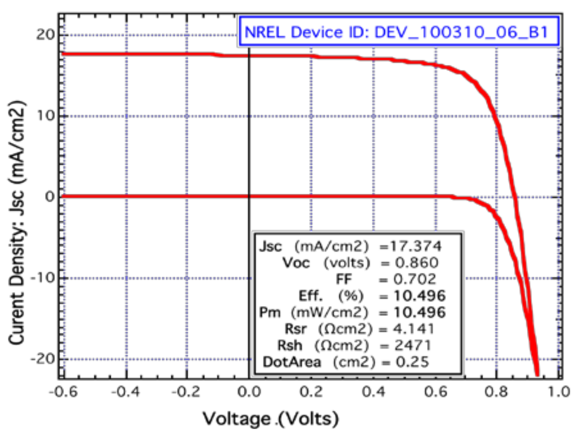
10.5% PECVD thin-film a-Si:H cell in 6-inch PDIL cluster tool

- Establishes quality for 6-inch industrial collaborations
- Key advance is p^+/p^- double layer

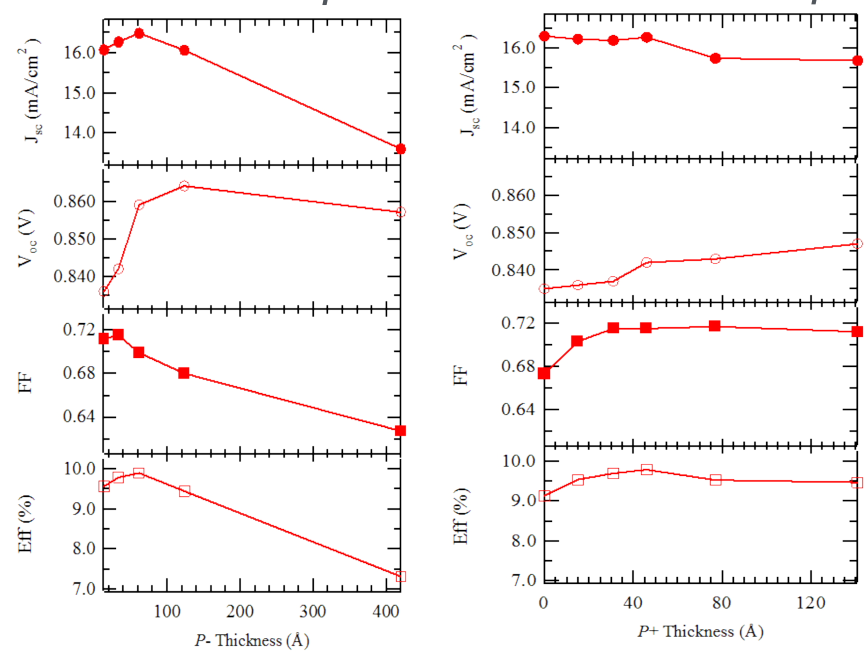
Q. Wang et al, in preparation



10.5% on 0.25 cm^2 cell:



- *p^+/p^-* -layer optimization



NREL Hot-Wire CVD epitaxy at high rate

U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

- Decomposition to Si, H at wire
  - React $Si + SiH_4$ ---> $Si_2H_2 + H_2$
  - Si_2H_2 deposition radical

  Zheng & Gallagher, TSF 2008

- Real-time spectroscopic ellipsometry
  - Layer-by-layer monitoring of crystallinity, thickness & roughness

  Teplin et al, JAP 2005

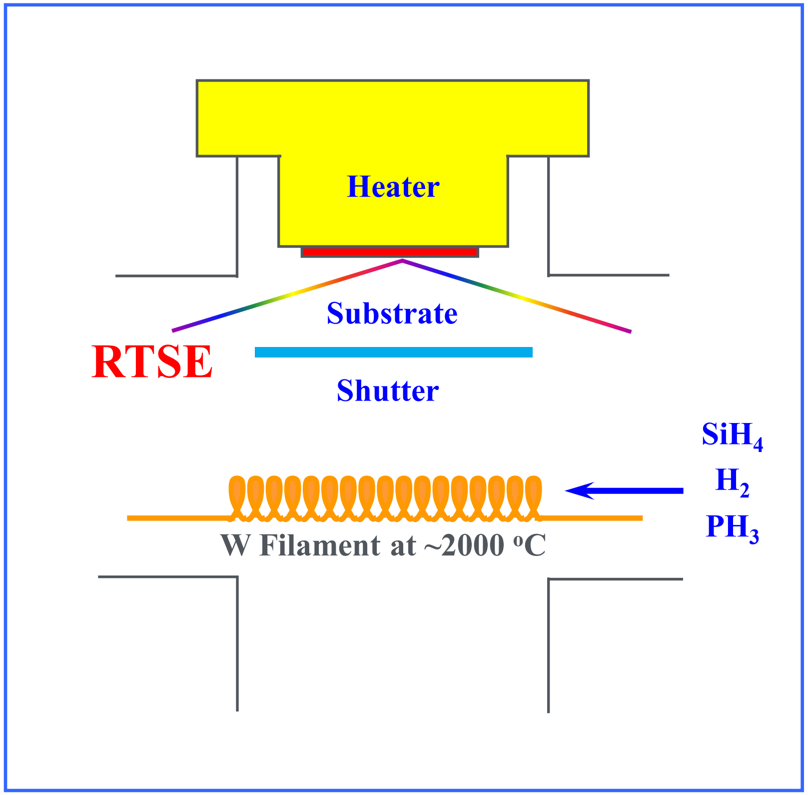
- Contolled n- and p-type doping

  Martin et al, TSF 2008

- Demonstrated 40-micron epitaxy

- High-rate 300 nm/min epitaxy
  - Can grow 3 micron PV absorber in 10 minutes
  - Increased wire area needed for micron per minute rate

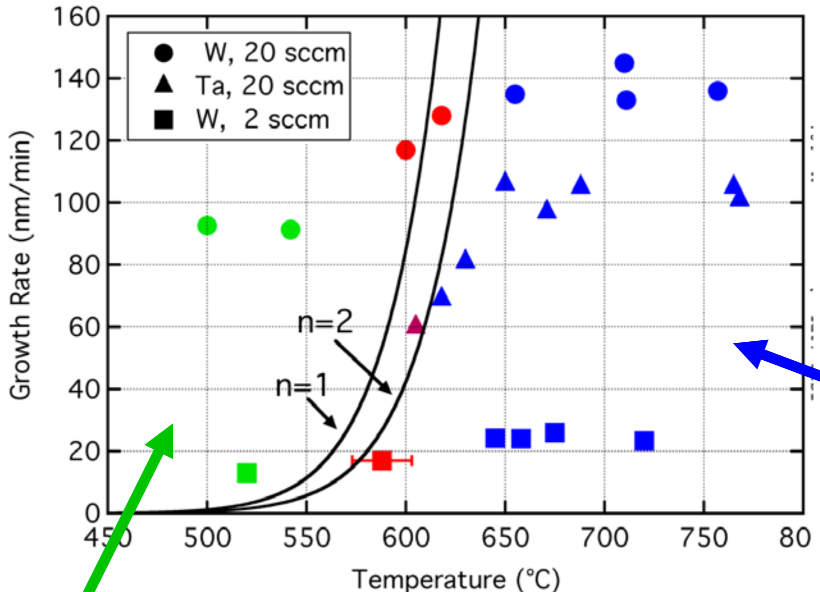
  Martin et al, JAP 2010

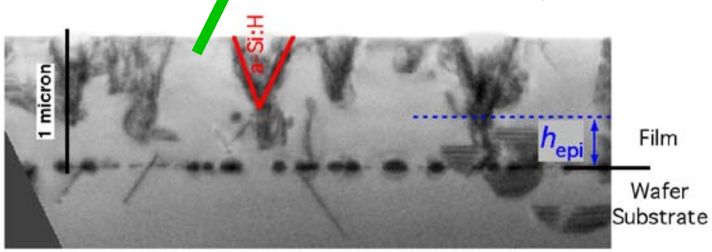


Mapped deposition phase space for thick HWCVD epitaxy

Epitaxy requires unhydrogenated surface sites

- Curves separate fully mono-hydride surface from surface with DBs
- Steady-state balance between H arrival and desorption





- SAD and high-res TEM confirm high-quality epitaxy

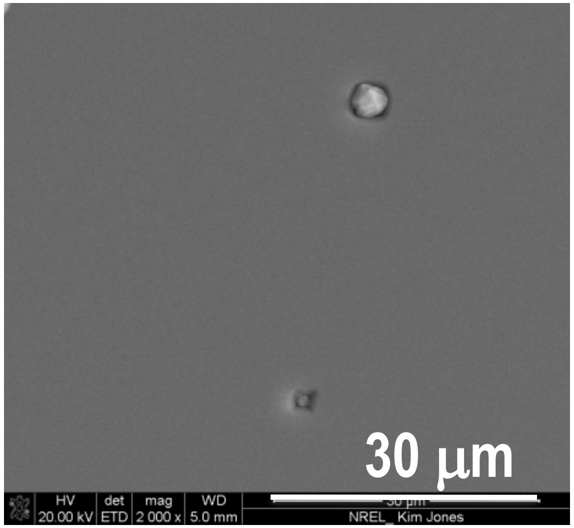
Teplin et al. APL, in press

Low defect density HWCVD epitaxy

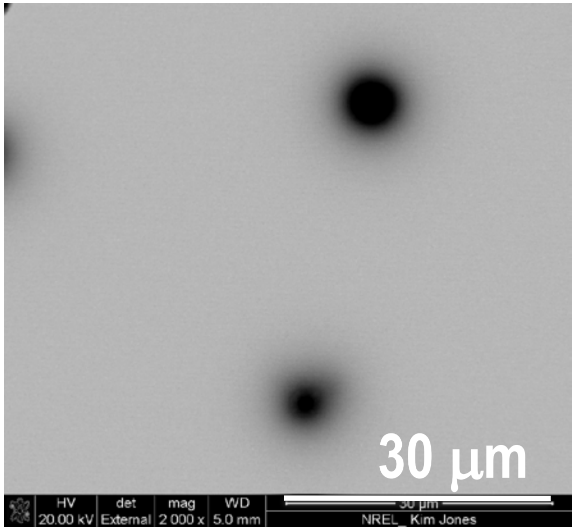
- Developed reliable methods of defect density counting
  - E-beam cathodoluminescence and EBIC of recombination-active defects
  - Low dislocation density confirmed at small areas by TEM

- Example: 10-micron thick solar cell with < 6 x 10^4 cm^{-2} defects

SEM



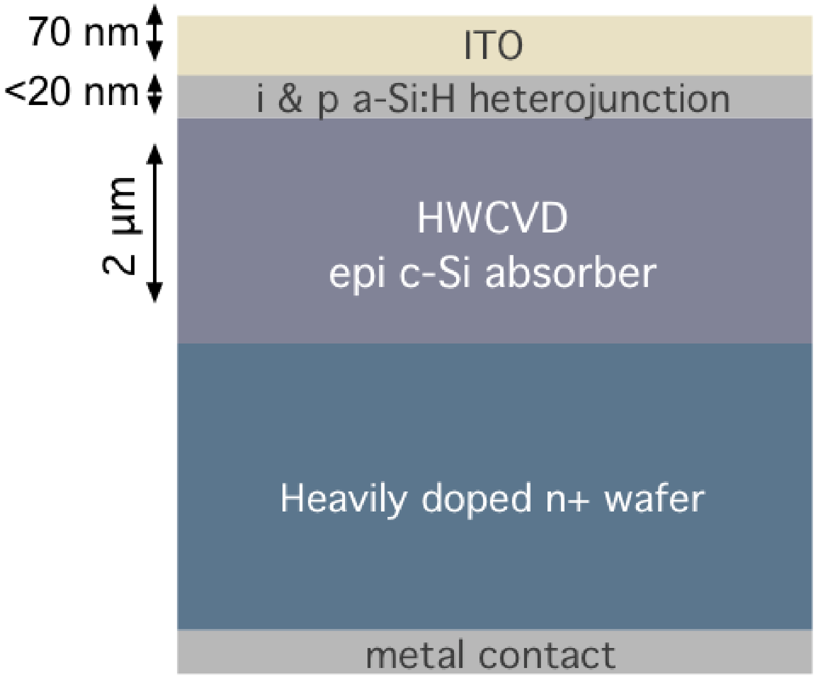
E-beam induced current (EBIC)

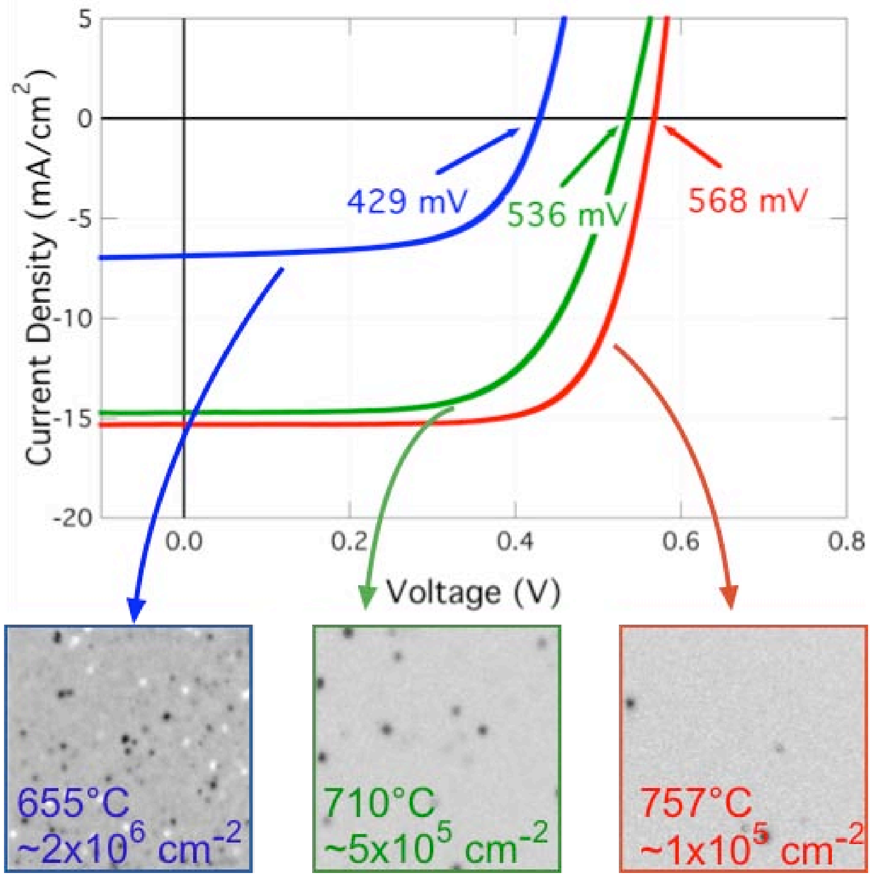


- 40-µm spacing between defects excellent for ~6 µm-thick absorber layer

Epitaxial quality supports V_{oc} of 568 mV

- Silicon heterojunction test devices on 'dead' wafer (wafer provides ~1 mA/cm^2)





- 6.3% efficiency with no light trapping, RTA or hydrogenation
- Dislocation density controls V_{oc}

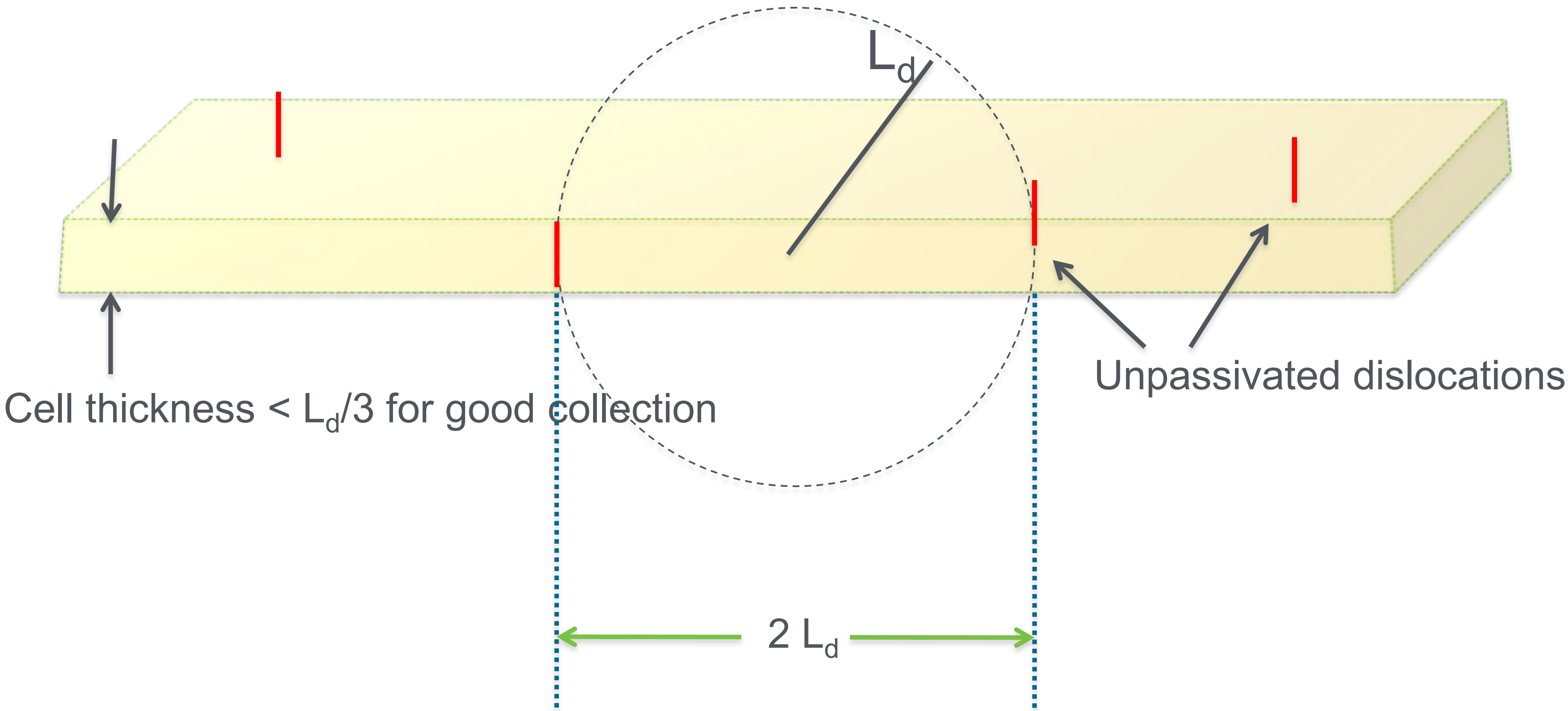
Alberi et al. APL, 2009

Analysis of test cells & PC1D models

U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

- IQE & dislocation measurements reveal quality requirement:
  - unpassivated dislocation spacing 6 times absorber thickness

Alberi et al, APL 2010



L_d limited to half the unpassivated dislocation spacing

Impurities:
Film c-Si is far more tolerant than wafer

U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

Alberi et al, APL 2010

Diffusion-limited cell (random walk) physics

Diffusion length, L:

$$\tau \sim \frac{1}{N} \qquad L \sim (D\tau)^{1/2} \sim N^{-1/2}$$

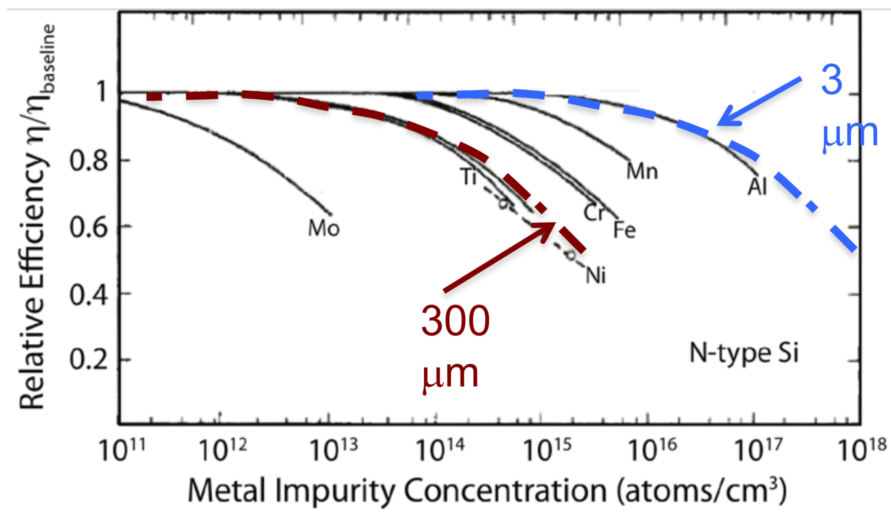
Max impurity level vs thickness, d

$$L > 3d \longrightarrow N_{max} \sim \frac{1}{(3d)^2}$$

Impurity tolerance, N_{max}

$$\frac{N_{max}(3\mu m)}{N_{max}(300\mu m)} \sim \frac{300^2}{3^2} \sim 10^4$$

Example: Ni tolerance in c-Si



Davis et al., IEEE Trans. Electron Devices, 1980

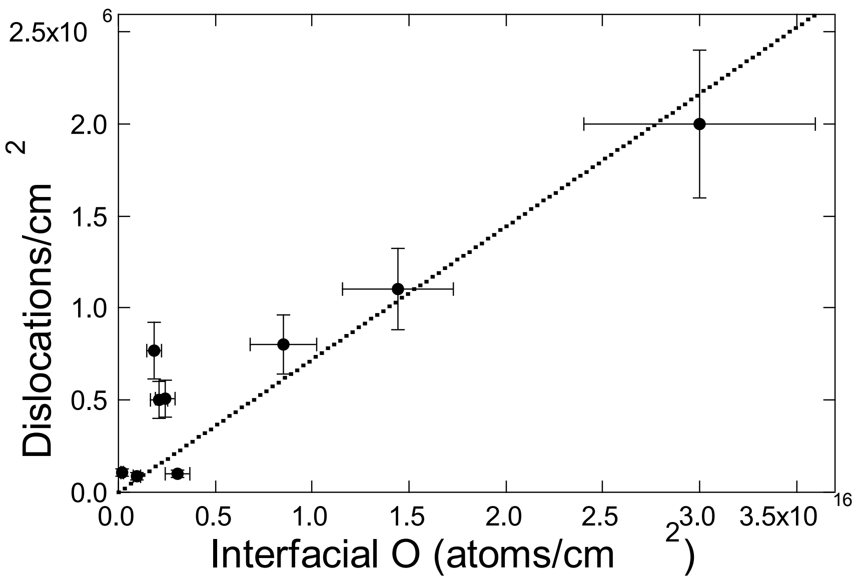
Dislocations are caused by O at surface and can be controlled

U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

- T-dependence of dislocation density matches suboxide desorption E_{act}

Teplin et al. APL, in press

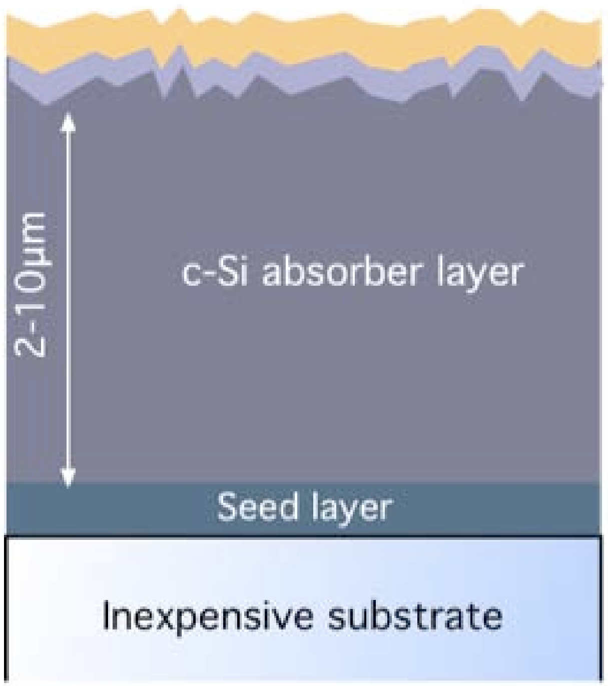
- SIMS shows dislocation correlation with interface oxygen



- We are perfecting surface-oxygen reduction methods
  - Already reduced dislocation density to $6x10^4$ cm^{-2} (> 45-μm spacing)

Martin et al. APL, in preparation

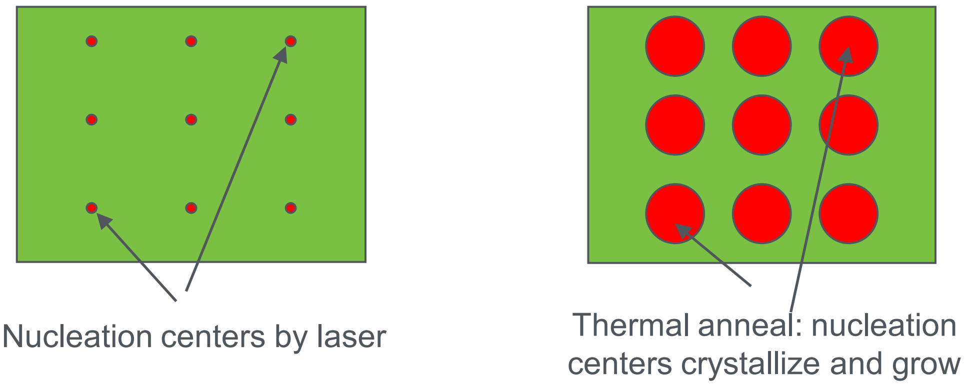
Seed layers initiate high-quality crystal growth



- Important seed layer properties
  - Large crystalline grains
  - Grains oriented coherently
    - (100) preferred
  - Low-angle grain boundaries
    - In-plane orientation of grains
  - If foreign, compatible with Si epitaxy
  - Few intragrain defects

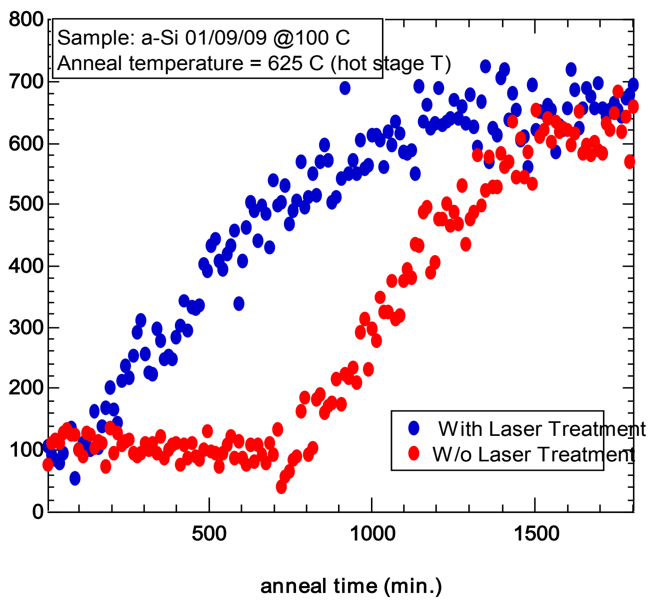
NREL seed layer project: Sub-threshold laser pretreat array

U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy



Dabney et al. APL, 2009

- Laser-pretreat amorphous silicon with sparse array of nucleation centers
  - Below threshhold for producing deleterious multicrystalline spots



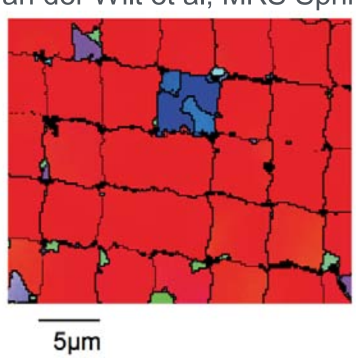
- FY09: Discovered laser treatment regime which speeds nucleation by factor of 7X

Next: Pretreat with sub-threshhold spot array to obtain large grains

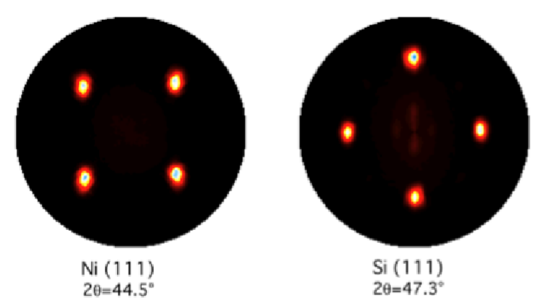
External collaborations for seed layers

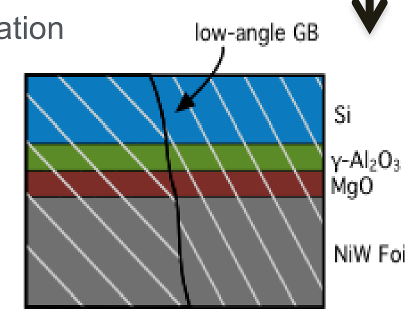
Partner	Type	Seed	Si epi?	PV cell
ORNL/Ampulse	Nat. Lab /Startup	Biaxial foreign on metal foil	Yes	Yes
Corning	Industry	Layer Transfer	Yes	Yes
Sharp	Industry	Layer Transfer	Yes	Yes
3 different partners	Industry	Proprietary	Yes (on first 1 of 3)	
Stanford	University	Biaxial foreign on glass	Awaiting suitable sample	
Columbia	University	Uniaxial laser Si on glass	In progress	

Electron back-scattered diffraction (EBSD)
van der Wilt et al, MRS Spring A, 2008



X-ray diffraction (111) pole figures
Heteroepitaxy with 45° in-plane rotation

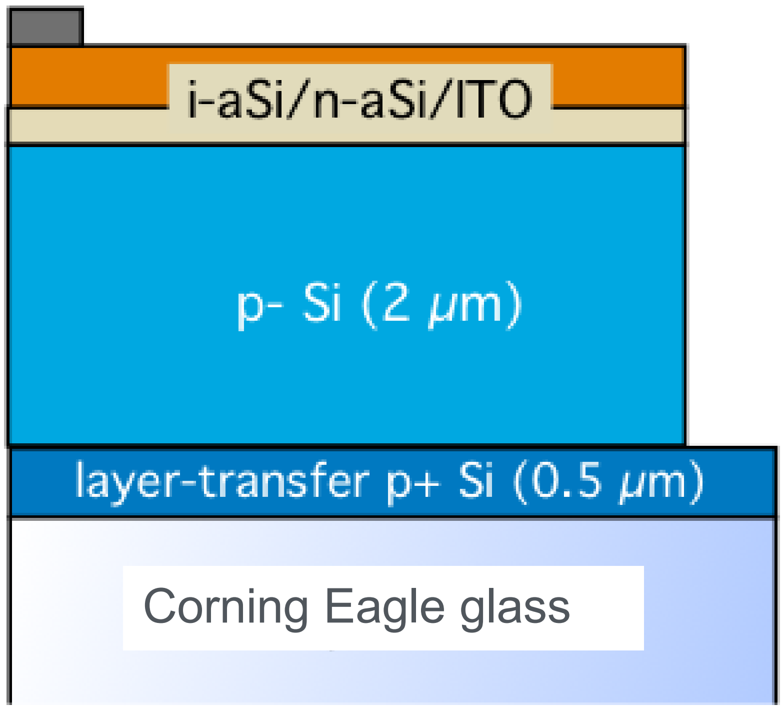


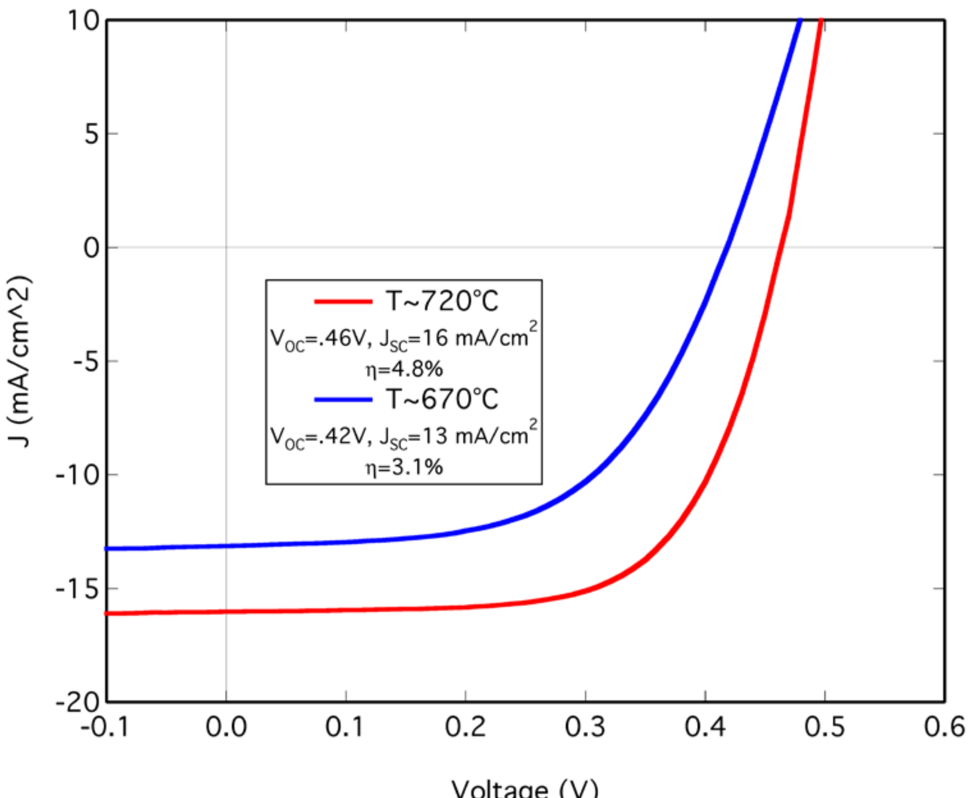


19

Late news: Proof-of-concept epitaxial solar cell

- Layer transfer Si seed on $26/m^2 Eagle glass + NREL HWCVD epitaxy
- 4.8% efficient without hydrogenation, RTP or light-trapping





Collaboration with E. Mozdy and T.K. Chuang, Corning

Future Plans

U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

- Implement improved low- defect density epitaxy in PV cells on glass
  - Raise layer-transfer 'ideal seed' voltage to > 600 mV
  - Validate PC1D models with thickness series
  - Apply wider range of RTP and hydrogenation conditions
- Evaluate quality of epitaxy and PV cells on newly-acquired seeds
  - Foreign templates
  - Laser-crystallized seeds
  - Proprietary industry seeds
- Down-select by September the least promising of NREL's 3 seed layer approaches
  - elimination of microwave anneal task is likely

- Planned FY11 Agreement changes
  - Epitaxy at high quality at higher rate and lower temperature
  - Continue developing only the most promising of NREL seed layers
  - Initiate formal light-trapping task to accelerate work and raise current density
  - Initiate exploratory task for proprietary alternate approach to wafer replacement
- FY13 goal is 15% cell on glass or metal foil
  - Challenge is to develop and integrate several unproven but critical techologies

Summary

- Film silicon: Wafer silicon efficiency in a thin-film cost structure
  - Avoids high $$ and energy costs of wafers
  - Abundant, non-toxic silicon for TW-scale PV
- > 15% achievable in 2-10 micron c-Si films
  - Seed layer & epitaxy for good crystal quality
  - Need spacing between dislocations at least 6 times thickness
- HW epitaxy on c-Si at display-glass-compatible T
  - 40-μm defect spacing (6 x 10^4 cm^{-2} dislocations)
  - Scalable 300 nm/min with path to micron per minute
- Proof-of-concept HWCVD epitaxial solar cells designed, fabricated, measured and modeled
  - On (dead) wafer with 568 mV
  - On display glass with 463 mV
- All the key barriers identified and can be surmounted
  - better epitaxy at higher rates, less expensive seeds, improved contacting, and good light-trapping

NREL Participants – Thank you

U.S. DEPARTMENT OF ENERGY | Energy Efficiency & Renewable Energy

- Kirstin Alberi
- Carolyn Beall
- Joe Berry
- Matt Dabney
- Anna Duda
- Harvey Guthrie
- Falah Hasoon
- Kim Jones
- Eugene Iwaniczko
- Harv Mahan
- Ina Martin
- Bill Nemeth
- Bob Reedy
- Manuel Romero
- Maxim Shub
- Paul Stradins
- Charles Teplin
- Qi Wang
- Yueqin Xu
- David Young